8A, 4MHz, Monolithic Synchronous Step-Down Regulator

FEATURES

- **High Efficiency: Up to 95%**
- **8A Output Current**
- **2.25V to 5.5V Input Voltage Range**
- **Low $R_{DS(ON)}$ Internal Switch: 35mΩ**
- **Tracking Input to Provide Easy Supply Sequencing**
- Programmable Frequency: 300kHz to 4MHz
- 0.8V ±1% Reference Allows Low Output Voltage
- Quiescent Current: 380µA
- Selectable Forced Continuous/Burst Mode® Operation with Adjustable Burst Clamp
- Synchronizable Switching Frequency
- Low Dropout Operation: 100% Duty Cycle
- Power Good Output Voltage Monitor
- Overtemperature Protected
- 38-Lead Low Profile (0.75mm) Thermally Enhanced QFN (5mm × 7mm) Package

APPLICATIONS

- Microprocessor, DSP and Memory Supplies
- Distributed 2.5V, 3.3V and 5V Power Systems
- Automotive Applications
- Point of Load Regulation
- Notebook Computers

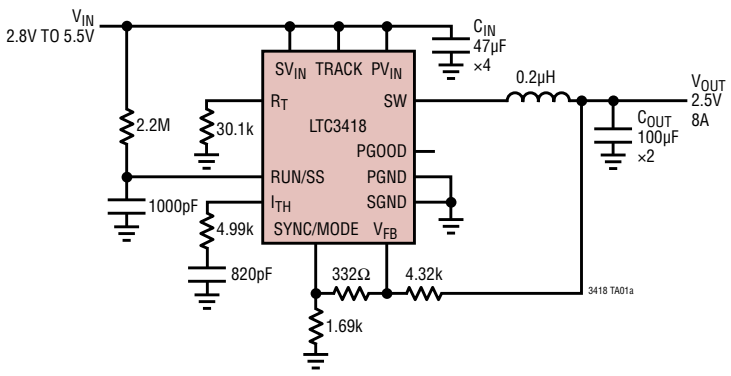
DESCRIPTION

The LTC®3418 is a high efficiency, monolithic synchronous step-down DC/DC converter utilizing a constant frequency, current mode architecture. It operates from an input voltage range of 2.25V to 5.5V and provides a regulated output voltage from 0.8V to 5V while delivering up to 8A of output current. The internal synchronous power switch increases efficiency and eliminates the need for an external Schottky diode. Switching frequency is set by an external resistor or can be synchronized to an external clock. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

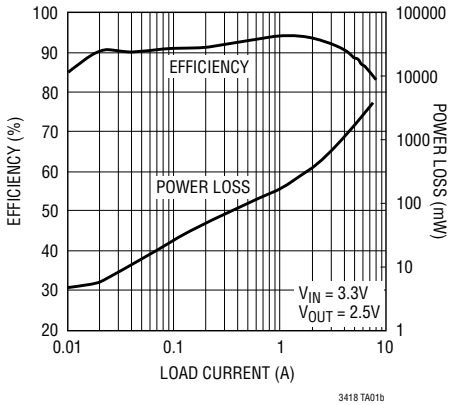
The LTC3418 can be configured for either Burst Mode operation or forced continuous operation. Forced continuous operation reduces noise and RF interference while Burst Mode operation provides high efficiency by reducing gate charge losses at light loads. In Burst Mode operation, external control of the burst clamp level allows the output voltage ripple to be adjusted according to the requirements of the application. A tracking input in the LTC3418 allows for proper sequencing with respect to another power supply.

TYPICAL APPLICATION

2.5V/8A Step-Down Regulator



Efficiency and Power Loss vs Load Current

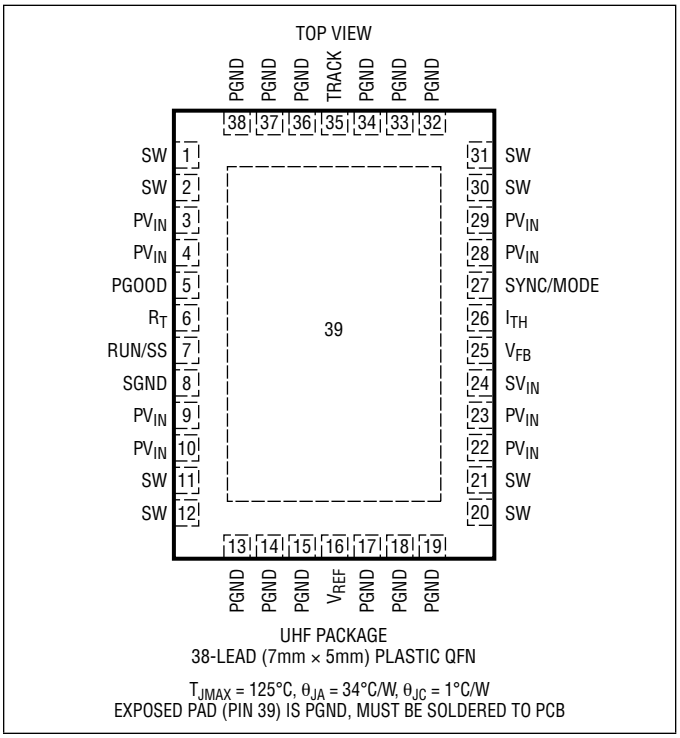


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage ..... –0.3V to 6V
I_{TH}, RUN/SS, V_{FB} Voltages ..... –0.3V to V_{IN}
SYNC/MODE Voltages ..... –0.3V to V_{IN}
TRACK Voltage ..... –0.3V to V_{IN}
SW Voltage ..... –0.3V to (V_{IN} + 0.3V)
Operating Temperature Range
(Note 2) .....–40°C to 85°C
Junction Temperature (Note 5) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (7mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W, θ_{JC} = 1°C/W
EXPOSED PAD (PIN 39) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC3418#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3418EUHF#PBF	LTC3418EUHF#TRPBF	3418	38-Lead (7mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range			2.25		5.5	V
V_{FB}	Regulated Feedback Voltage	0°C ≤ T_A ≤ 85°C (Note 3)	 ●	0.792 0.784	0.800 0.800	0.808 0.816	V V
I_{FB}	Feedback Input Current				100	200	nA
ΔV_{FB}	Reference Voltage Line Regulation	V_{IN} = 2.5V to 5.5V (Note 3)			0.04	0.2	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	Measured in Servo Loop, V_{ITH} = 0.36V Measured in Servo Loop, V_{ITH} = 0.84V	● ●		0.02 –0.02	0.2 –0.2	% %
V_{TRACK}	Tracking Voltage Offset	V_{TRACK} = 0.4V				15	mV
	Tracking Voltage Range			0		0.8	V
I_{TRACK}	TRACK Input Current				100	200	nA
ΔV_{PGOOD}	Power Good Range				±7.5	±9	%
R_{PGOOD}	Power Good Resistance				100	150	Ω
I_Q	Input DC Bias Current Active Current Shutdown	(Note 4) V_{FB} = 0.7V, V_{ITH} = 1V V_{RUN} = 0V			 380 0.03	 450 1.5	 µA µA
f_{OSC}	Switching Frequency Switching Frequency Range	R_{OSC} = 69.8kΩ (Note 6)		0.88 0.3	1	1.12 4	MHz MHz
f_{SYNC}	SYNC Capture Range	(Note 6)		0.3		4	MHz
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW} = 600mA			35	50	mΩ
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW} = –600mA			25	35	mΩ
I_{LIMIT}	Peak Current Limit			12	17		A
V_{UVLO}	Undervoltage Lockout Threshold			1.75	2	2.25	V
V_{REF}	Reference Output			1.219	1.250	1.281	V
I_{LSW}	SW Leakage Current	V_{RUN} = 0V, V_{IN} = 5.5V			0.1	1	µA
V_{RUN}	RUN Threshold			0.5	0.65	0.8	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3418 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The LTC3418 is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage (I_{TH}).

Note 4: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

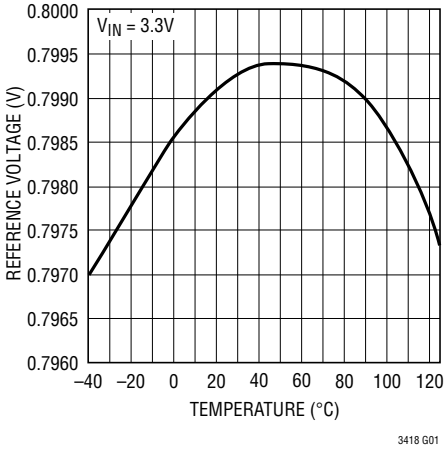
Note 5: T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

LTC3418: $T_J = T_A + (P_D)(34°C/W)$

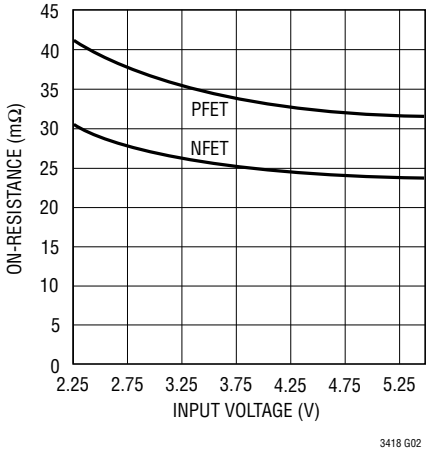
Note 6: This parameter is guaranteed by design and characterization.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

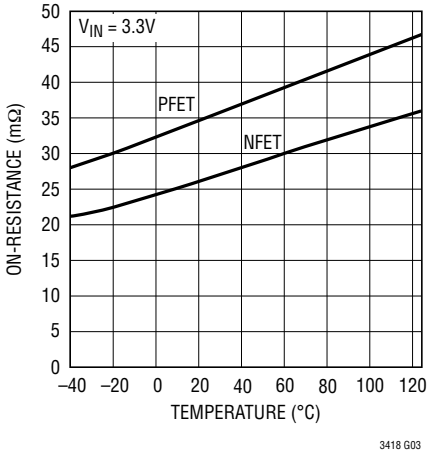
Internal Reference Voltage vs Temperature



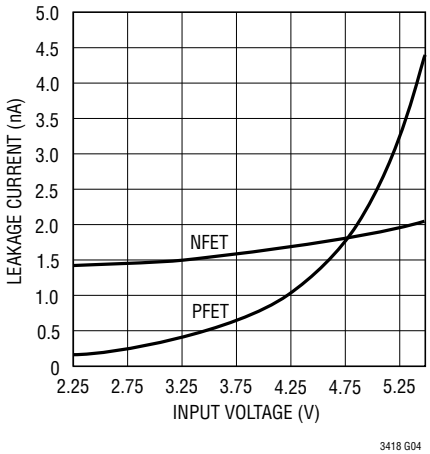
Switch On-Resistance vs Input Voltage



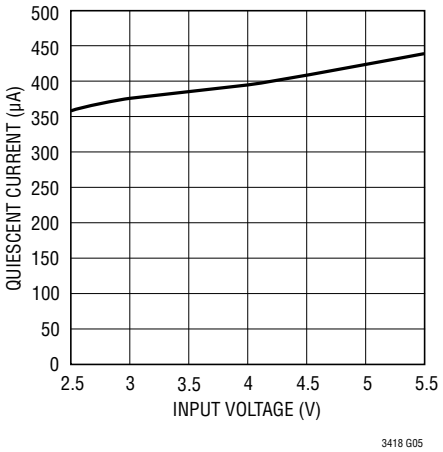
On-Resistance vs Temperature



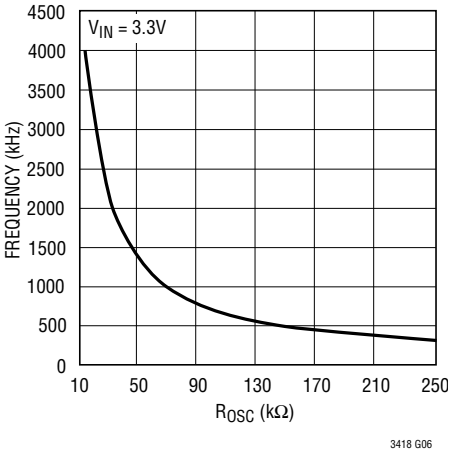
Switch Leakage vs Input Voltage



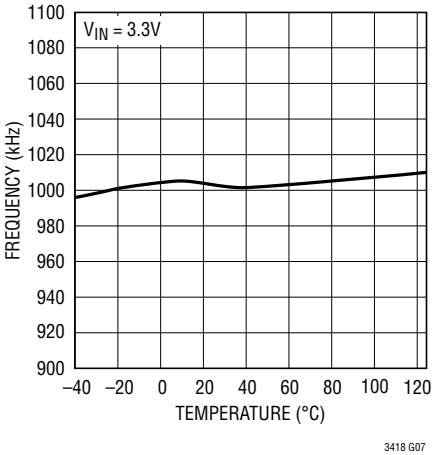
Quiescent Current vs Input Voltage



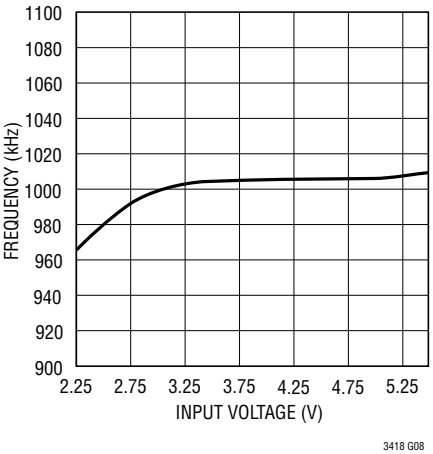
Frequency vs R_{OSC}



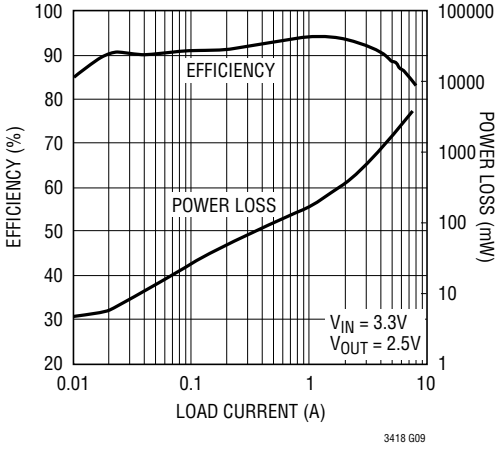
Frequency vs Temperature



Frequency vs Input Voltage

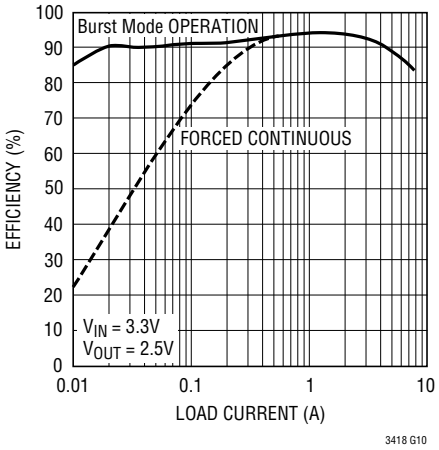


Efficiency and Power Loss vs Load Current

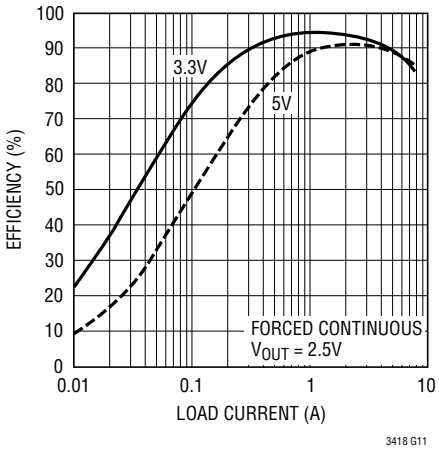


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

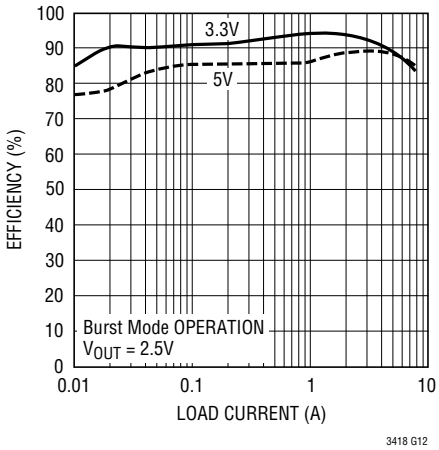
Efficiency vs Load Current



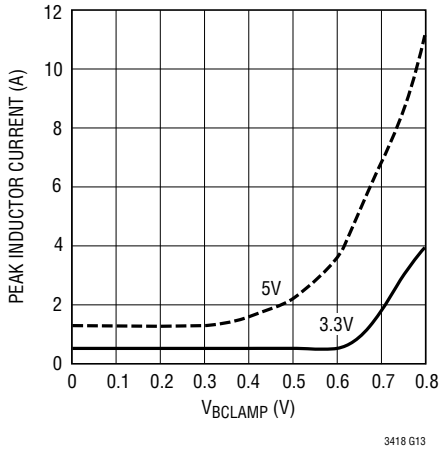
Efficiency vs Load Current



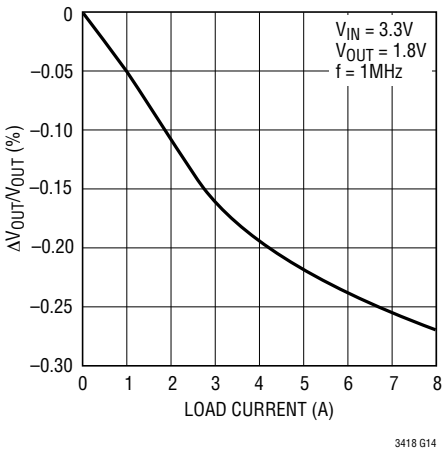
Efficiency vs Load Current



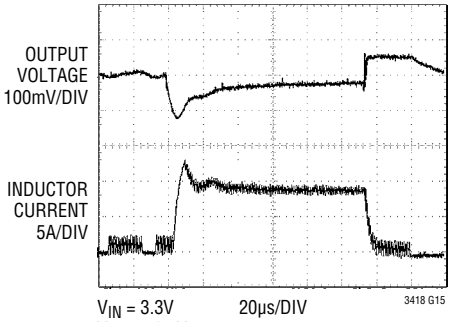
Peak Inductor Current vs Burst Clamp Voltage



Load Regulation

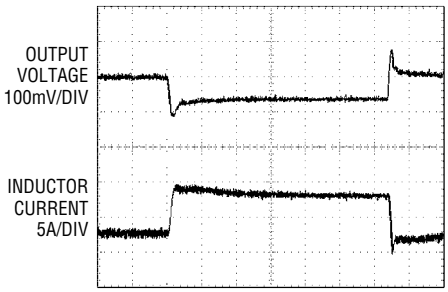


Load Step Transient



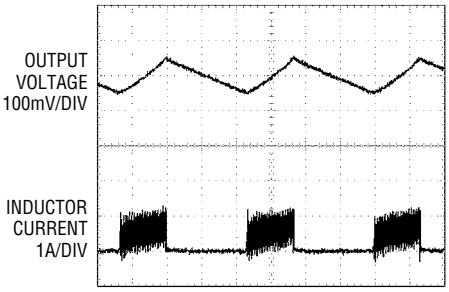
VIN = 3.3V 20µs/DIV
VOUT = 2.5V
LOAD STEP: 800mA TO 8A

Load Step Transient



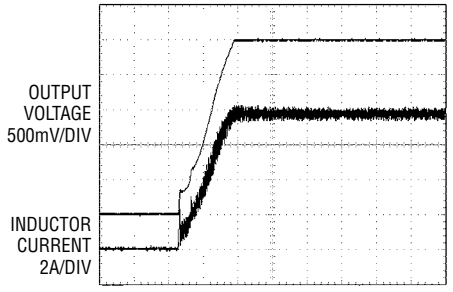
VIN = 3.3V 40µs/DIV
VOUT = 2.5V
LOAD STEP: 3A TO 8A

Burst Mode Operation



VIN = 3.3V 20µs/DIV
VOUT = 2.5V
LOAD: 200mA

Start-Up Transient



VIN = 3.3V 1ms/DIV
VOUT = 2.5V
LOAD: 8A

PIN FUNCTIONS

SW (Pins 1, 2, 11, 12, 20, 21, 30, 31): Switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

PV_{IN} (Pins 3, 4, 9, 10, 22, 23, 28, 29): Power Input Supply. Decouple these pins to PGND with capacitors on all four corners of the package.

PGOOD (Pin 5): Power Good Output. Open-drain logic output that is pulled to ground when the output voltage is not within ±7.5% of regulation point.

R_T (Pin 6): Oscillator Resistor Input. Connecting a resistor to ground from this pin sets the switching frequency.

RUN/SS (Pin 7): Run Control and Soft-Start Input. Forcing this pin below 0.5V shuts down the LTC3418. In shutdown all functions are disabled drawing <1.5µA of supply current. A capacitor to ground from this pin sets the ramp time to full output current.

SGND (Pin 8): Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point.

PGND (Pins 13, 14, 15, 17, 18, 19, 32, 33, 34, 36, 37, 38): Power Ground. Connect this pin closely to the (–) terminal of C_{IN} and C_{OUT}.

V_{REF} (Pin 16): Reference Output. Decouple this pin with a 2.2µF capacitor.

SV_{IN} (Pin 24): Signal Input Supply. Decouple this pin to SGND with a capacitor.

V_{FB} (Pin 25): Feedback Pin. Receives the feedback voltage from a resistive divider connected across the output.

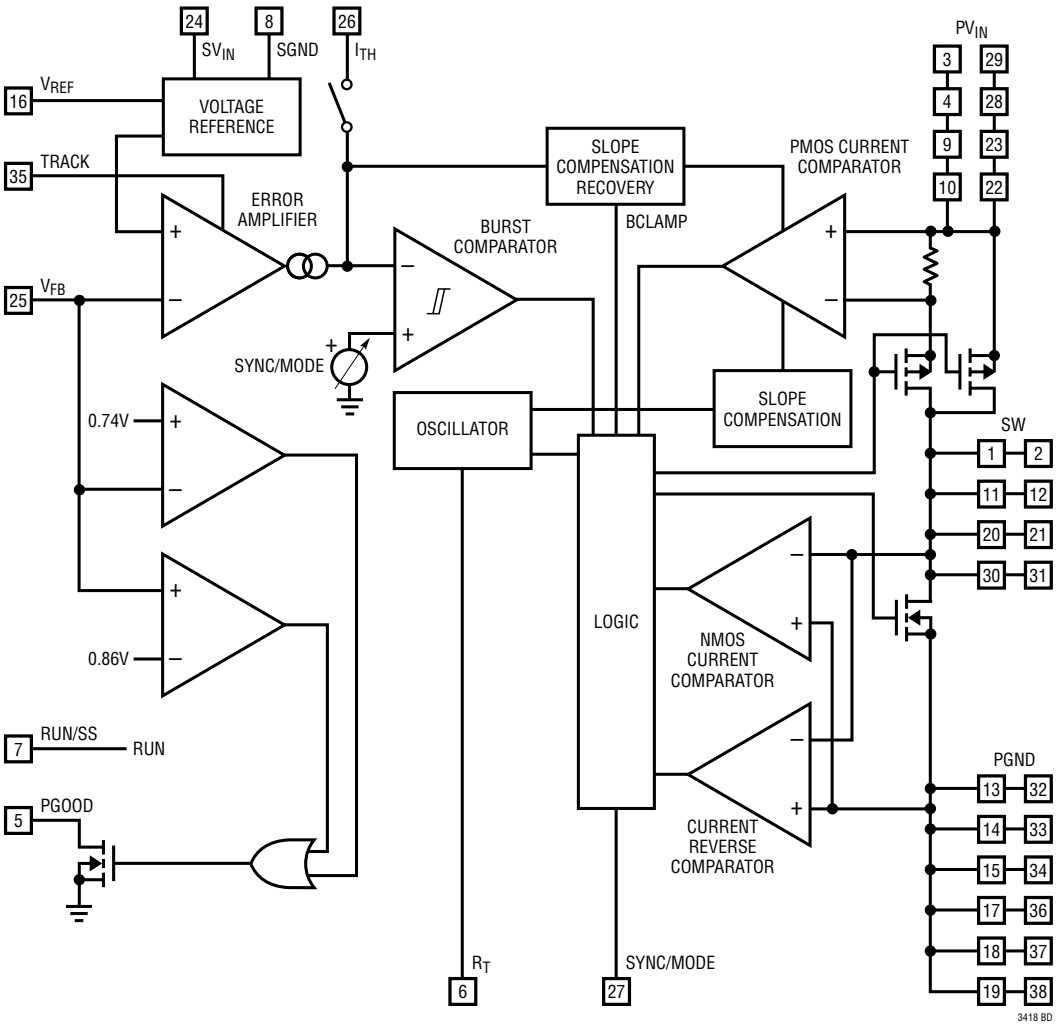
I_{TH} (Pin 26): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is from 0.2V to 1.4V with 0.4V corresponding to the zero-sense voltage (zero current).

SYNC/MODE (Pin 27): Mode Select and External Clock Synchronization Input. To select Forced Continuous, tie to SV_{IN}. Connecting this pin to a voltage between 0V and 1V selects Burst Mode operation with the burst clamp set to the pin voltage.

TRACK (Pin 35): Voltage Tracking Input. Feedback voltage will regulate to the voltage on this pin during start-up power sequencing.

Exposed Pad (Pin 39): The Exposed Pad is PGND and must be soldered to the PCB ground for electrical connection and rated thermal performance.

BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3418 is a monolithic, constant frequency, current mode step-down DC/DC converter. During normal operation, the internal top power switch (P-channel MOSFET) is turned on at the beginning of each clock cycle. Current in the inductor increases until the current comparator trips and turns off the top power MOSFET. The peak inductor current at which the current comparator shuts off the top power switch is controlled by the voltage on the I_{TH} pin. The error amplifier adjusts the voltage on the I_{TH} pin by comparing the feedback signal from a resistor divider on the V_{FB} pin with an internal 0.8V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier raises the I_{TH} voltage until the average inductor current matches the new load current. When the top power MOSFET shuts off, the synchronous power switch (N-channel MOSFET) turns on until either the bottom current limit is reached or the beginning of the next clock cycle. The bottom current limit is set at –8A for force continuous mode and 0A for Burst Mode operation.

The operating frequency is externally set by an external resistor connected between the R_T pin and ground. The practical switching frequency can range from 300kHz to 4MHz.

Overvoltage and undervoltage comparators will pull the PGOOD output low if the output voltage comes out of regulation by ±7.5%. In an overvoltage condition, the top power MOSFET is turned off and the bottom power MOSFET is switched on until either the overvoltage condition clears or the bottom MOSFET's current limit is reached.

Forced Continuous

Connecting the SYNC/MODE pin to SV_{IN} will disable Burst Mode operation and force continuous current operation. At light loads, forced continuous mode operation is less efficient than Burst Mode operation, but may be desirable in some applications where it is necessary to keep switching harmonics out of a signal band. The output voltage ripple is minimized in this mode.

Burst Mode Operation

Connecting the SYNC/MODE pin to a voltage in the range of 0V to 1V enables Burst Mode operation. In Burst Mode operation, the internal power MOSFETs operate intermittently at light loads. This increases efficiency by minimizing switching losses. During Burst Mode operation, the minimum peak inductor current is externally set by the voltage on the SYNC/MODE pin and the voltage on the I_{TH} pin is monitored by the burst comparator to determine when sleep mode is enabled and disabled. When the average inductor current is greater than the load current, the voltage on the I_{TH} pin drops. As the I_{TH} voltage falls below 350mV, the burst comparator trips and enables sleep mode. During sleep mode, the top power MOSFET is held off while the load current is solely supplied by the output capacitor. When the output voltage drops, the top and bottom power MOSFETs begin switching to bring the output back into regulation. This process repeats at a rate that is dependent on the load demand.

Pulse skipping operation can be implemented by connecting the SYNC/MODE pin to ground. This forces the burst clamp level to be at 0V. As the load current decreases, the peak inductor current will be determined by the voltage on the I_{TH} pin until the I_{TH} voltage drops below 400mV. At this point, the peak inductor current is determined by the minimum on-time of the current comparator. If the load demand is less than the average of the minimum on-time inductor current, switching cycles will be skipped to keep the output voltage in regulation.

Frequency Synchronization

The internal oscillator of the LTC3418 can by synchronized to an external clock connected to the SYNC/MODE pin. The frequency of the external clock can be in the range of 300kHz to 4MHz.

For this application, the oscillator timing resistor should be chosen to correspond to a frequency that is 25% lower than the synchronization frequency. During synchronization, the burst clamp is set to 0V, and each switching cycle begins at the falling edge of the clock signal.

OPERATION

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle eventually reaching 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-channel MOSFET and the inductor.

Low Supply Operation

The LTC3418 is designed to operate down to an input supply voltage of 2.25V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-channel and N-channel power switches increases. The user should calculate the power dissipation when the LTC3418 is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal. Normally, the maximum inductor peak current is reduced when slope compensation is added. In the LTC3418, however, slope compensation recovery is implemented to keep the maximum inductor peak current constant throughout the range of duty cycles. This keeps the maximum output current relatively constant regardless of duty cycle.

Short-Circuit Protection

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. To prevent current runaway from occurring, a secondary current limit is imposed on the inductor current. If the inductor valley current increases larger than 15A, the top power MOSFET will be held off and switching cycles will be skipped until the inductor current is reduced.

Voltage Tracking

Some microprocessors and DSP chips need two power supplies with different voltage levels. These systems often require voltage sequencing between the core power supply and the I/O power supply. Without proper sequencing, latch-up failure or excessive current draw may occur that could result in damage to the processor's I/O ports or the I/O ports of a supporting system device such as memory, an FPGA or a data converter. To ensure that the I/O loads are not driven until the core voltage is properly biased, tracking of the core supply and the I/O supply voltage is necessary.

Voltage tracking is enabled by applying a ramp voltage to the TRACK pin. When the voltage on the TRACK pin is below 0.8V, the feedback voltage will regulate to this tracking voltage. When the tracking voltage exceeds 0.8V, control over the feedback voltage is gradually released. Full release of tracking control over the feedback voltage is achieved when the tracking voltage exceeds 1.05V.

Voltage Reference Output

The LTC3418 provides a 1.25V reference voltage that is capable of sourcing up to 5mA of output current. This reference voltage is generated from a linear regulator and is intended for applications requiring a low noise reference voltage. To ensure that the output is stable, the reference voltage pin should be decoupled with a minimum of 2.2µF.

APPLICATIONS INFORMATION

The basic LTC3418 application circuit is shown on the front page of this data sheet. External component selection is determined by the maximum load current and begins with the selection of the operating frequency and inductor value followed by C_{IN} and C_{OUT}.

Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency of the LTC3418 is determined by an external resistor that is connected between the R_T pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_{OSC} = \frac{7.3 \cdot 10^{10}}{f}\left[\Omega\right] - 2.5k\Omega$$

Although frequencies as high as 4MHz are possible, the minimum on-time of the LTC3418 imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 80ns. Therefore, the minimum duty cycle is equal to:

100 • 80ns • f(Hz)

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} or V_{OUT} and decreases with higher inductance:

$$\Delta I_L = \left(\frac{V_{OUT}}{fL}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces the core losses in the inductor, the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f\Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor value will also have an effect on Burst Mode operation. The transition from low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

APPLICATIONS INFORMATION

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coiltronics, Coilcraft, Toko and Sumida.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the source of the top MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.8 \left(1 + \frac{R2}{R1} \right)$$

The resistive divider allows pin V_{FB} to sense a fraction of the output voltage as shown in Figure 1.

APPLICATIONS INFORMATION

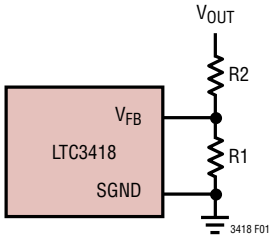


Figure 1. Setting the Output Voltage

Burst Clamp Programming

If the voltage on the SYNC/MODE pin is less than V_{IN} by 1V, Burst Mode operation is enabled. During Burst Mode operation, the voltage on the SYNC/MODE pin determines the burst clamp level, which sets the minimum peak inductor current, I_{BURST}, for each switching cycle. A graph showing the relationship between the minimum peak inductor current and the voltage on the SYNC/MODE pin can be found in the Typical Performance Characteristics section. In the graph, V_{BURST} is the voltage on the SYNC/MODE pin. I_{BURST} can only be programmed in the range of 0A to 10A. For values of V_{BURST} less than 0.4V, I_{BURST} is set at 0A. As the output load current drops, the peak inductor currents decrease to keep the output voltage in regulation. When the output load current demands a peak inductor current that is less than I_{BURST}, the burst clamp will force the peak inductor current to remain equal to I_{BURST} regardless of further reductions in the load current. Since the average inductor current is greater than the output load current, the voltage on the I_{TH} pin will decrease. When the I_{TH} voltage drops to 350mV, sleep mode is enabled in which both power MOSFETs are shut off and switching action is discontinued to minimize power consumption. All circuitry is turned back on and the power MOSFETs begin switching again when the output voltage drops out of regulation. The value for I_{BURST} is determined by the desired amount of output voltage ripple. As the value of I_{BURST} increases, the sleep period between pulses and the output voltage ripple increase. The burst clamp voltage, V_{BURST}, can be set by a resistor divider from the V_{FB} pin to the SGND pin as shown in the Typical Application on the front page of this data sheet.

Pulse skipping, which is a compromise between low output voltage ripple and efficiency during low load current operation, can be implemented by connecting the SYNC/MODE pin to ground. This sets I_{BURST} to 0A. In this condition, the peak inductor current is limited by the minimum on-time of the current comparator; and the lowest output voltage ripple is achieved while still operating discontinuously. During very light output loads, pulse skipping allows only a few switching cycles to be skipped while maintaining the output voltage in regulation.

Voltage Tracking

The LTC3418 allows the user to program how its output voltage ramps during start-up by means of the TRACK pin. Through this pin, the output voltage can be set up to either track coincidentally or ratiometrically follow another output voltage as shown in Figure 2. If the voltage on the TRACK pin is less than 0.8V, voltage tracking is enabled. During voltage tracking, the output voltage regulates to the tracking voltage through a resistor divider network.

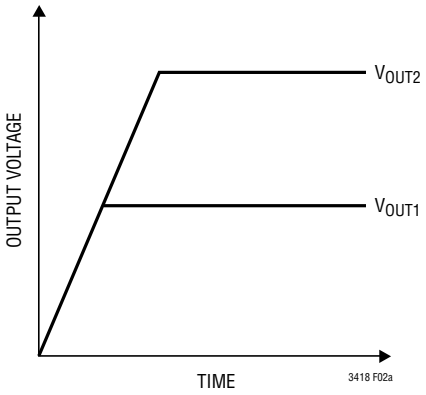


Figure 2a. Coincident Tracking

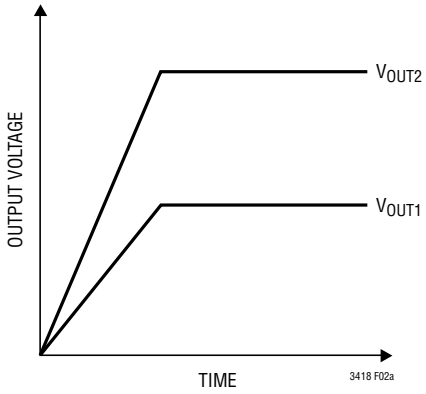


Figure 2b. Ratiometric Sequencing

APPLICATIONS INFORMATION

The output voltage during tracking can be calculated with the following equation:

$$V_{OUT} = V_{TRACK}\left(1+\frac{R2}{R1}\right), V_{TRACK} < 0.8V$$

To implement the coincident tracking in Figure 2a, connect an extra resistor divider to the output of V_{OUT2} and connect its midpoint to the TRACK pin of the LTC3418 as shown in Figure 3. The ratio of this divider should be selected the same as that of V_{OUT1}'s resistor divider. To implement the ratiometric sequencing in Figure 2b, the extra resistor divider's ratio should be set so that the TRACK pin voltage exceeds 1.05V by the end of the start-up period. The LTC3418 utilizes a method in which the TRACK pin's control over the output voltage is gradually released as the TRACK pin voltage approaches 0.8V. With this technique, some overdrive will be required on the TRACK pin to ensure that the tracking function is completely disabled at the end of the start-up period.

For coincident tracking, the following condition should be satisfied to ensure that tracking is disabled at the end of start-up.

$$V_{OUT2} \geq 1.32\ V_{OUT1}$$

For ratiometric tracking, the following equation can be used to calculate the resistor values:

$$R4 = R3\left(\frac{V_{OUT2}}{V_{TRACK}} - 1\right)$$

$$V_{TRACK} \geq 1.05V$$

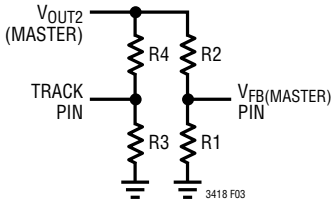


Figure 3

Frequency Synchronization

The LTC3418's internal oscillator can be synchronized to an external clock signal. During synchronization, the top MOSFET turn-on is locked to the falling edge of the external frequency source. The synchronization frequency range is 300kHz to 4MHz. Synchronization only occurs if the external frequency is greater than the frequency set by the external resistor. Because slope compensation is generated by the oscillator's RC circuit, the external frequency should be set 25% higher than the frequency set by the external resistor to ensure that adequate slope compensation is present.

Soft-Start

The RUN/SS pin provides a means to shut down the LTC3418 as well as a timer for soft-start. Pulling the RUN/SS pin below 0.5V places the LTC3418 in a low quiescent current shutdown state (I_Q < 1.5µA).

The LTC3418 contains a soft-start clamp that can be set externally with a resistor and capacitor on the RUN/SS pin as shown in Typical Application on the front page of this data sheet. The soft-start duration can be calculated by using the following formula:

$$t_{SS} = R_{SS} \bullet C_{SS} \bullet \ln\frac{V_{IN}}{V_{IN} - 1.8V}[\text{Seconds}]$$

When the voltage on the RUN/SS pin is raised above 2V, the full current range becomes available on I_{TH}.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} quiescent current and I^2R losses.

The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load

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currents can be misleading since the actual power lost is of no consequence.

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the Electrical Characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.
2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Thermal Considerations

In most applications, the LTC3418 does not dissipate much heat due to its high efficiency.

But, in applications where the LTC3418 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the LTC3418 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = (P_D)(\theta_{JA})$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. For the 38-Lead 5mm × 7mm QFN package, the θ_{JA} is 34°C/W.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$).

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current.

When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD}(ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. The I_{TH} pin external components and output capacitor shown in the Typical Application on the front page of this data sheet will provide adequate compensation for most applications.

Design Example

As a design example, consider using the LTC3418 in an application with the following specifications: V_{IN} = 3.3V, V_{OUT} = 2.5V, $I_{OUT(MAX)}$ = 8A, $I_{OUT(MIN)}$ = 200mA, f = 1MHz. Because efficiency is important at both high and low load current, Burst Mode operation will be utilized.

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First, calculate the timing resistor:

$$R_{OSC} = \frac{7.3 \cdot 10^{10}}{1 \cdot 10^{6}} - 2.5k = 70.5k$$

Use a standard value of 69.8k. Next, calculate the inductor value for about 40% ripple current:

$$L = \left(\frac{2.5V}{(1MHz)(3.2A)}\right)\left(1 - \frac{2.5V}{3.3V}\right) = 0.19\mu H$$

Using a 0.2µH inductor results in a maximum ripple current of:

$$\Delta I_L = \left(\frac{2.5V}{(1MHz)(0.2\mu H)}\right)\left(1 - \frac{2.5V}{3.3V}\right) = 3.03A$$

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, five 100µF ceramic capacitors will be used.

C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = (8A)\left(\frac{2.5V}{3.3V}\right)\sqrt{\frac{3.3V}{2.5V} - 1} = 3.43A_{RMS}$$

Decoupling the PV_{IN} and SV_{IN} pins with four 100µF capacitors is adequate for this application.

The burst clamp and output voltage can now be programmed by choosing the values of R1, R2 and R3. The voltage on the MODE pin will be set to 0.67V by the resistor divider consisting of R2 and R3. A burst clamp voltage of 0.67V will set the minimum inductor current, I_{BURST}, to approximately 1.2A.

If we set the sum of R2 and R3 to 200k, then the following equations can be solved.

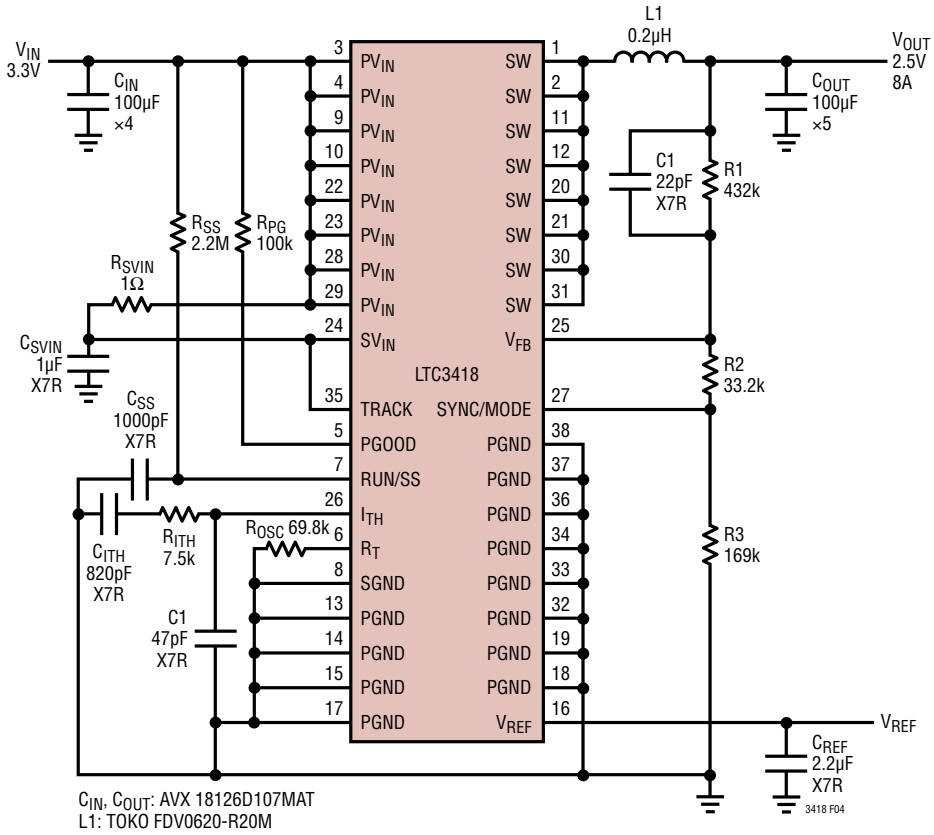


Figure 4. 2.5V, 8A Regulator at 1MHz, Burst Mode Operation

APPLICATIONS INFORMATION

$$R2 + R3 = 200k$$

$$1 + \frac{R2}{R3} = \frac{0.8V}{0.67V}$$

The two equations shown above result in the following values for R2 and R3: R2 = 33.2k, R3 = 169k. The value of R1 can now be determined by solving the equation:

$$1 + \frac{R1}{202.2k} = \frac{2.5V}{0.8V}$$

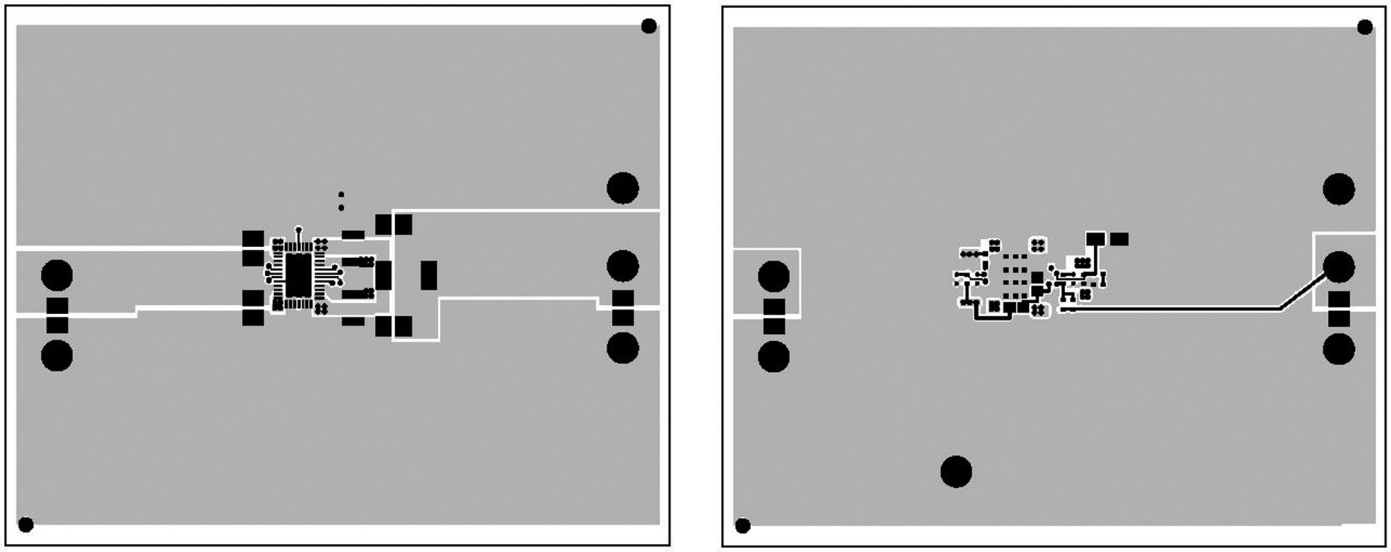
$$R1 = 430k$$

A value of 432k will be selected for R1. Figure 4 shows the complete schematic for this design example.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3418. Check the following in your layout.

1. A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small-signal components returning to the SGND pin at one point which is then connected to the PGND pin close to the LTC3418.
2. Connect the (+) terminals of the input capacitor(s), C_{IN}, as close as possible to the PV_{IN} and PGND pins at all four corners of the package. These capacitors provide the AC current into the internal power MOSFETs.
3. Keep the switching node, SW, away from all sensitive small-signal nodes.
4. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. You can connect the copper areas to any DC net (PV_{IN}, SV_{IN}, V_{OUT}, PGND, SGND or any other DC rail in your system).
5. Connect the V_{FB} pin directly to the feedback resistors. The resistor divider must be connected between V_{OUT} and SGND.
6. To minimize switching noise coupling to SV_{IN}, place an optional local filter between SV_{IN} and PV_{IN}. Most designs do not require this filter.

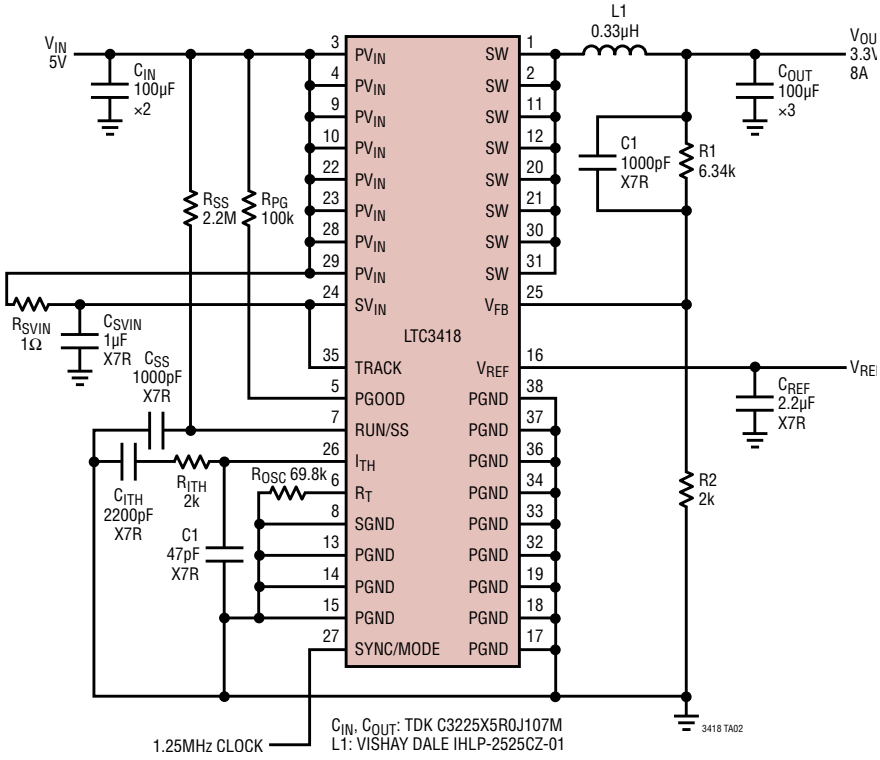


Top Layer Bottom Layer

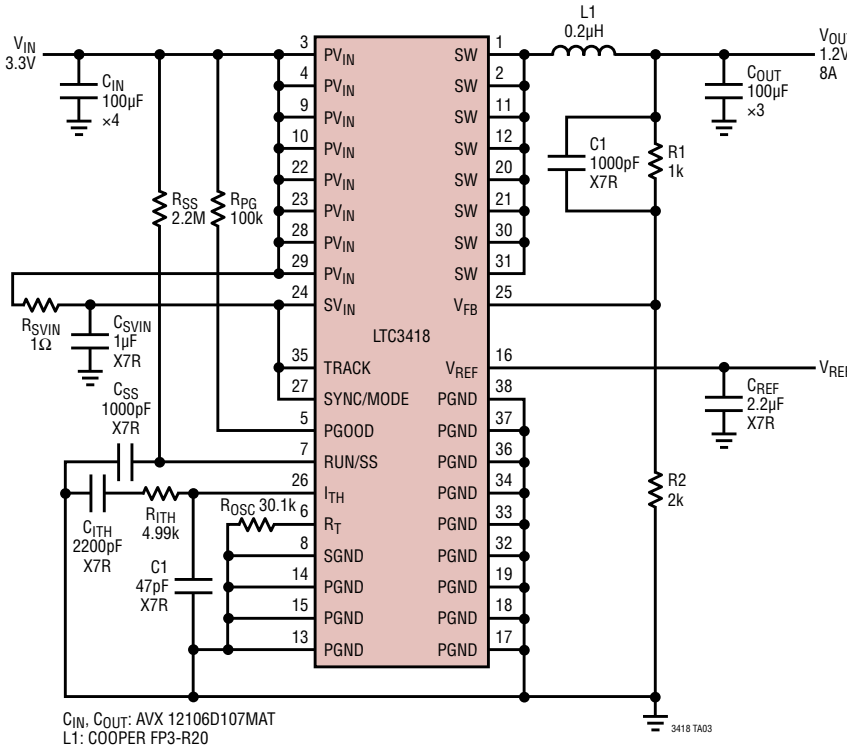
Figure 5. LTC3418 Layout Diagram

TYPICAL APPLICATIONS

3.3V, 8A Step-Down Regulator Synchronized to 1.25MHz

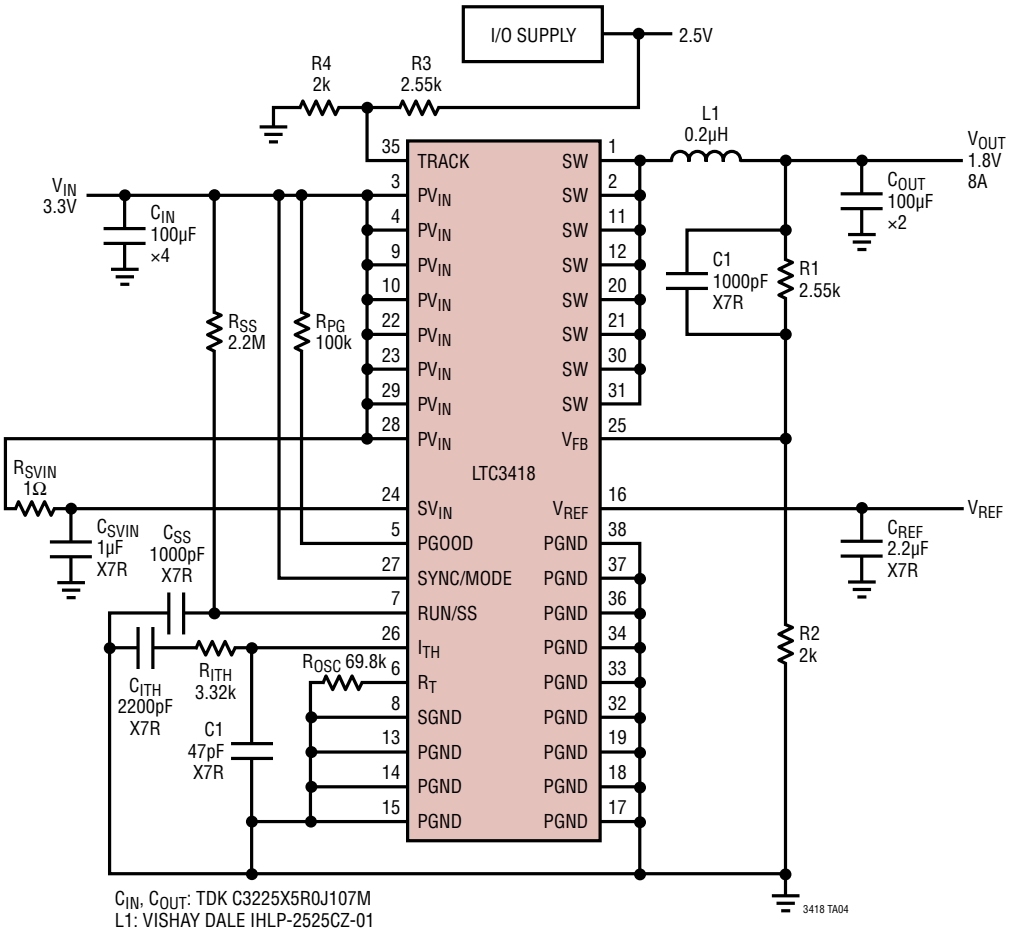


1.2V, 8A Step-Down Regulator at 2MHz, Forced Continuous Mode



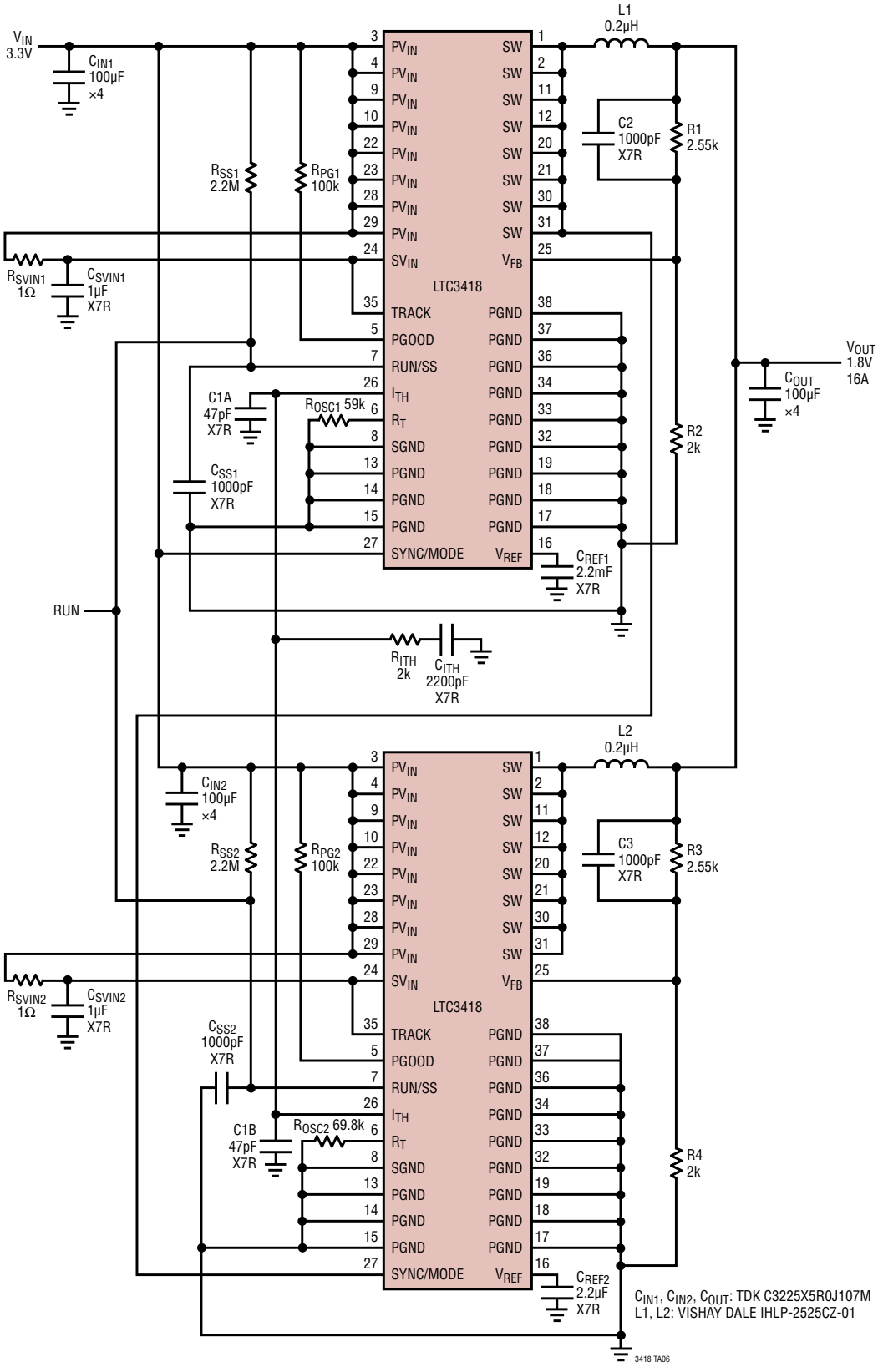
TYPICAL APPLICATIONS

1.8V, 8A Step-Down Regulator with Tracking



TYPICAL APPLICATIONS

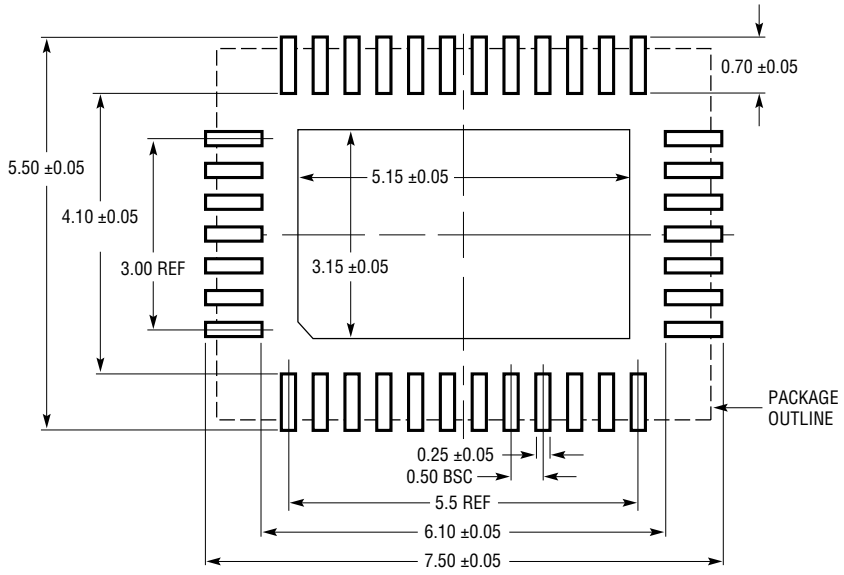
1.8V, 16A Step-Down Regulator



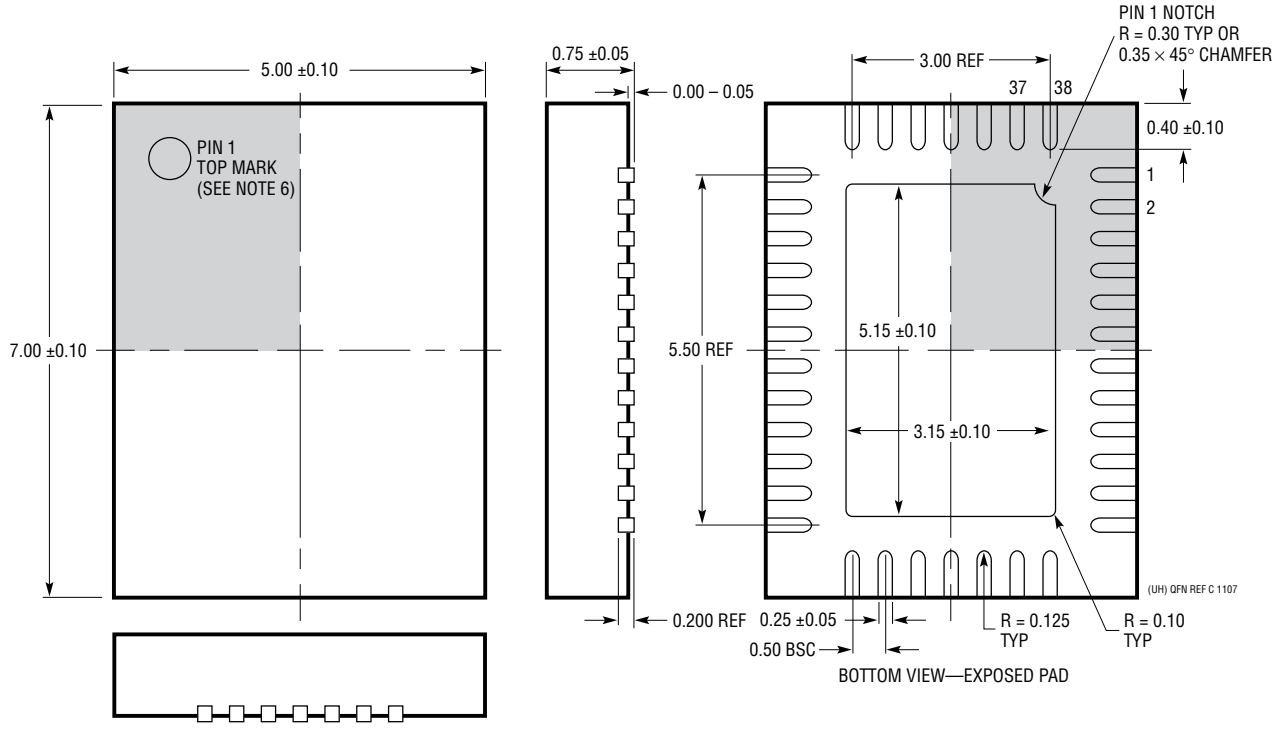
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3418#packaging for the most recent package drawings.

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



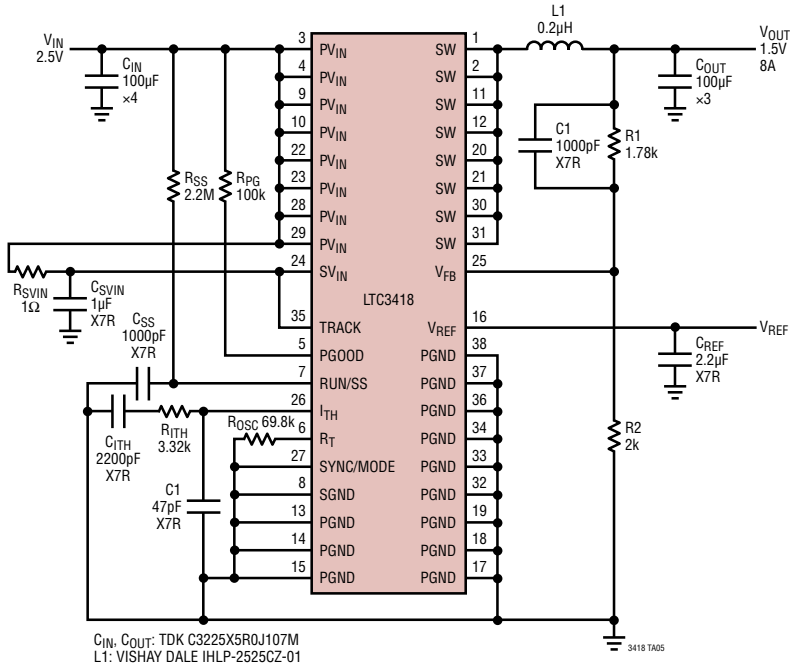
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	1/17	Modified Application Circuits	19, 22

TYPICAL APPLICATION

Low Noise 1.5V, 8A Step-Down Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1616	500mA (I_{OUT}), 1.4MHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN}: 3.6V to 25V, V_{OUT} = 1.25V, I_Q = 1.9mA, I_{SD} < 1µA, ThinSOT Package
LT1676	450mA (I_{OUT}), 100kHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN}: 7.4V to 60V, V_{OUT} = 1.24V, I_Q = 3.2mA, I_{SD} < 2.5µA, S8 Package
LT1765	25V, 2.75A (I_{OUT}), 1.25MHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN}: 3V to 25V, V_{OUT} = 1.2V, I_Q = 1mA, I_{SD} < 15µA, S8, TSSOP16E Packages
LTC1879	1.20A (I_{OUT}), 550kHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.7V to 10V, V_{OUT} = 0.8V, I_Q = 15µA, I_{SD} < 1µA, TSSOP16 Package
LTC3405/LTC3405A	300mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.75V to 6V, V_{OUT} = 0.8V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3406/LTC3406B	600mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, V_{OUT} = 0.6V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3407	Dual 600mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, V_{OUT} = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MS Package
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, V_{OUT} = 0.8V, I_Q = 60µA, I_{SD} < 1µA, MS Package
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, V_{OUT} = 0.8V I_Q = 60µA, I_{SD} < 1µA, TSSOP16E Package
LTC3413	3A (I_{OUT} Sink/source), 2MHz, Monolithic Synchronous Regulator for DDR/QDR Memory Termination	90% Efficiency, V_{IN}: 2.25V to 5.5V, V_{OUT} = V_{REF}/2, I_Q = 280µA, I_{SD} < 1µA, TSSOP16E Package
LTC3414	4A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, I_{SD} < 1µA, TSSOP20E Package
LTC3416	4A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter with Tracking	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 300µA, I_{SD} < 1µA, TSSOP20E Package

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